



PART B — (5 × 13 = 65 marks)

11. (a) With neat diagram, enumerate in detail the DC characteristics of CMOS inverter. (13)

Or

- (b) (i) Analyze the switching characteristics of a CMOS inverter. Derive rise time, fall time and propagation delay. (6)
- (ii) If two CMOS inverters are cascaded with an aspect ratio of 1:1 then determine the inverter-pair delay. (7)
12. (a) (i) Design a half adder using static CMOS logic. (6)
- (ii) Design a 4:1 MUX using 2:1 MUX. Realize it using transmission gate. (7)

Or

- (b) Realize a 2-input NOR gate using static CMOS logic, Domino logic and Complementary pass transistor logic. Analyze the hardware complexity in terms of transistor count. (13)
13. (a) (i) Enumerate in detail on the design of pulse registers. (6)
- (ii) Give in detail, the design and working of astable sequential circuits. (7)

Or

- (b) (i) Design a master-slave positive edge triggered D-flipflop using transmission gate. (6)
- (ii) Discuss on sense amplifier based registers. (7)
14. (a) Describe the hardware architecture of a 4-bit signed array multiplier. (13)

Or

- (b) (i) Elaborate in detail the design of a 4-bit barrel shifter. (6)
- (ii) Describe the working of 6-transistor SRAM cell. (7)

15. (a) Explain in detail the basic architecture of FPGA with a neat diagram. (13)

Or

- (b) Enumerate in detail the working of
- (i) Adhoc Test (5)
  - (ii) Scan based Test (8)

PART C — (1 × 15 = 15 marks)

16. (a) Apply Radix-2 booth encoding to perform multiplication between two 8-bit numbers (-5) and 4. (15)

Or

- (b) (i) Design a 4-bit carry look ahead adder using dynamic CMOS logic by deriving the necessary expressions. (6)
- (ii) Design a 3-bit even parity generator using NAND gates only. Design the circuit using static CMOS logic. (9)
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